The Silicon Radio Decade

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Invited Paper

***Abstract*—During the 1990s, we witnessed a string of advances in silicon RF integration: from the introduction of the first integrated silicon bipolar radios for groupe special mobile and digital European cordless telephone in the late 1980s toward full single-chip integration capabilities based on silicon–germanium BiCMOS technologies. Where RF design used to be a black art, it is becoming a “normal practice” today. In this paper, the authors are looking back on then years of circuits, silicon technology, and system research with roots in standardization and a scope reaching from the early ideas to the final product success on the market and some perspective toward new concepts and systems. The past decade was a turbulent period with new technologies popping up, dreams of RF CMOS gradually coming to reality, products in bipolar and GaAs and conferences crowded with RF papers. Too many to read or reread, but we summarize here what we remember still clearly after ten years and we try to look ahead in the near future.**

I. Introduction

In THE LATE 1980s, silicon bipolar RF technologies were maturing and provided n-p-n transistors with a transit frequency f_T of about 10 GHz. The poly-emitter transistor with the As shallow emitter junction placed in an implanted base and contacted by polysilicon was the motor for the introduction of silicon bipolar technology in the emerging cellular phone applications. An f_T of 10 GHz was just enough to create the basic transceiver functions for cellular applications with a carrier frequency below 1 GHz. The Gilbert cell mixer in a 5-V RF bipolar technology was a key circuit to integrate the RF transceivers for heterodyne and homodyne radio telephones. Later, during the 1990s, the f_T in silicon bipolar RF technologies increased to 20 and 30 GHz thanks to the introduction of trench isolation and silicidized poly for emitter and base and to the progress in lithography to submicrometer dimensions. A transit frequency f_T of 30 GHz is about the limit for today’s n-p-n silicon bipolar devices, even with selective implanted collectors. This limit is determined by the vertical diffusion depth of the base and the mobility of the carriers, which limit the base transit time.

Inspired by the heterobipolar approach in GaAs technologies with superior RF performance, germanium was introduced to realize heterojunctions in the silicon base. This is shown in Figs. 1 and 2: a germanium profile is superimposed on the p-type base implant. Two approaches are generally applied. In a first approach, a graded germanium profile is creating an electric field in the base region to accelerate the carriers that are diffusing from the emitter to the collector junction. In the second approach, a constant germanium doping over the base layer is realized to increase the mobility of the minority carriers in the base and to reduce the base resistance. Both approaches result in a higher f_T and a lower base resistance.

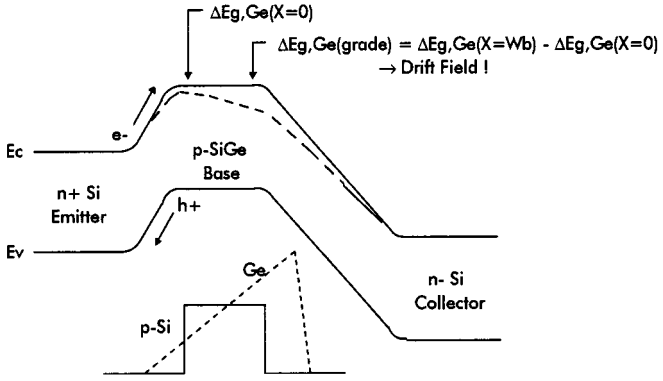

Fig. 1. Electron potential in the heterojunction bipolar SiGe transistor.

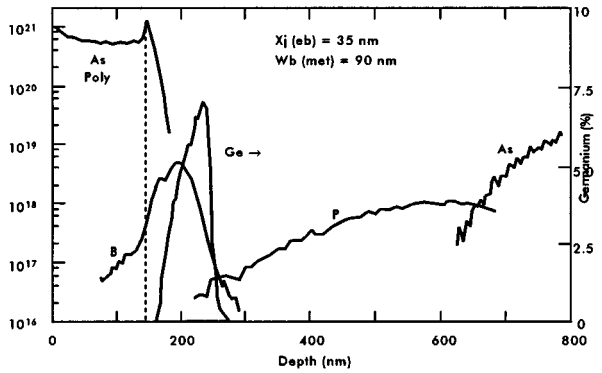

Fig. 2. Doping profile of SiGe heterojunction bipolar transistor.

Some research groups implanted the germanium in the silicon, while others did a co-deposition of silicon and germanium with chemical vapor deposition or similar epitaxial techniques. Co-deposition of the silicon and the germanium base layer is today considered as the most successful technique. The implanted approach still has attractive advantages, but suffers from the lattice damage as a result of the large germanium atoms implanted in between the silicon. Typically about 10–20 germanium atoms are implanted per 100 silicon atoms.

The silicon–germanium (SiGe) n-p-n transistor is currently in production in several foundries. The growing market for RF

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wireless integration is convincing the silicon foundries to invest in high-performance RF silicon technologies rather than in GaAs because of the compatibility of the silicon technologies with the main stream CMOS fabrication equipment.

Several emerging applications such as Universal Mobile Telecom System (UMTS) or wireless local area network (LAN) use higher carrier frequencies up to 5 GHz. For these applications, transistors with an f_T in the order of 50 GHz will be needed. SiGe is advantageous for these applications because of the higher f_T, but also because of the lower base resistance resulting in a lower transmit noise and a higher receiver sensitivity. The applications below 2 GHz will exploit the SiGe performance to fully integrate the radio function on a single chip and to eliminate the discrete components on the radio printed circuit board (PCB).

Historically, RF design was the art of s-parameters, shielding, impedance matching, and standing-wave ratios. Modern silicon radio-frequency integrated circuits (RFICs) are designed using the same SPICE-like tools as in low-frequency (LF) analog integrated circuits (ICs) with the addition of important software for system-level simulation and mixer circuit noise analysis. New RF design practices step away from the 50-Ω culture. Novel chip architectures, as well as powerful technological advances, are driving radio integration toward the ultimate single-chip phone. The obstacles in this quest are the stringent system requirements on noise figure, substrate crosstalk, and parasitic coupling, rather than the limitations of the silicon IC technology.

II. RFIC Fundamentals

In the last decade of this millennium, a new and exciting RF circuit capability became available as complete radio front-end ICs were developed in silicon bipolar and BiCMOS technologies. Such chips are widely used in cellular phones, global positioning system devices, and similar "low-gigahertz-band" products. These highly integrated radio parts represent an important new niche for IC manufacturers.

The original source for the creation of this new RFIC niche can be traced back to two events that took place approximately ten years ago. First, the progress in silicon bipolar IC technology, as described above, yielded transistors with approximately 10-GHz transition frequency. Since these devices were readily fabricated in low-cost silicon production facilities, the IC industry pushed the development of a new market for this technology. Second, the worldwide telecommunication industry became strongly motivated to spread the use of the mobile digital phone. This device became a consumer fashion. Together with several synergetic technological and economic forces, these conditions rapidly created the modern advanced radio products that are commonplace today.

In 1989, the groupe special mobile (GSM) and European Telecom Specification Institute (ETSI) wrote the specifications for the GSM system. In parallel, the semiconductor industry was working on submicrometer bipolar, CMOS and BiCMOS technologies. In the late 1980s, the first CMOS baseband analog and digital chips for the first-generation GSM handset were fabricated in a 1.2-μm CMOS technology. However, the technology road map for the following five years was

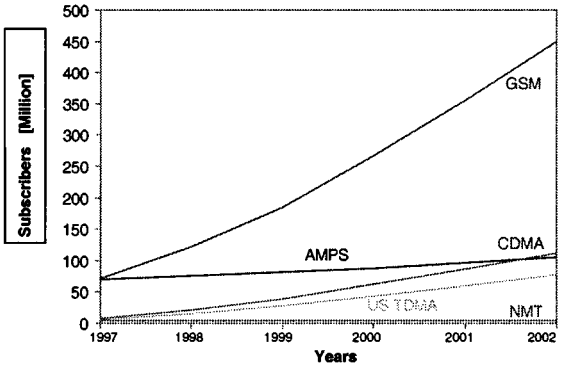

Fig. 3. World subscriber evolution per wireless standard.

projecting the transfer of submicrometer silicon technologies from solid-state research laboratories to reliable engineering and production. The silicon IC technology, GSM system engineering, application-specific integrated circuit (ASIC) design, the system software, and the commercial market for cellular phones were growing in a harmonic environment orchestrated by the European commission and the telecommunication industry.

RF design for applications below 2 GHz moved from the PCB with discrete components to large-scale integration in silicon technology. Time was ready for the creation of a new generation of engineers: RF ASIC or silicon monolithic-microwave integrated-circuit (MMIC) designers. In the early 1980s, the gigahertz spectrum had been GaAs territory, but at the end of that decade, the silicon technology conquered the cellular market for the transmit/receive mixers, while GaAs technology kept its presence in LNAs and power amplifiers (PAs). The high-level applications for military and space above 10 GHz remained primarily relying on GaAs technology. However, at the horizon, one could see how the silicon bipolar RF technology with self-aligned emitters and selectively implanted collectors was moving up to 30-GHz transition frequencies and above, while the use of the SiGe base could push that figure-of-merit to 100 GHz [1].

The production volumes for cellular phones had to grow massively to match the demand illustrated in Fig. 3. Today, the major successful companies for telecommunication consumer products are each manufacturing 20 million or more cellular phones per year. In Europe and other places, the number of digital cellular phones has reached a level that rivals the number of plain old wired telephones. Meanwhile, similar capabilities are being developed in Japan and the U.S. The worldwide compatibility of the UMTS will refuel this dramatic expansion.

III. New Directions

The pioneering days for the silicon bipolar RFICs are over, but the quest for an even more advanced radio remains. The single-chip cellular phone, the multistandard phone, the software radio, and the UMTS mobile broad-band communication phone are new challenges. We look at these targets with optimism because, just like ten years ago, the same economical and technological factors are present. The mobile telecommunication application and the silicon technology improvements are

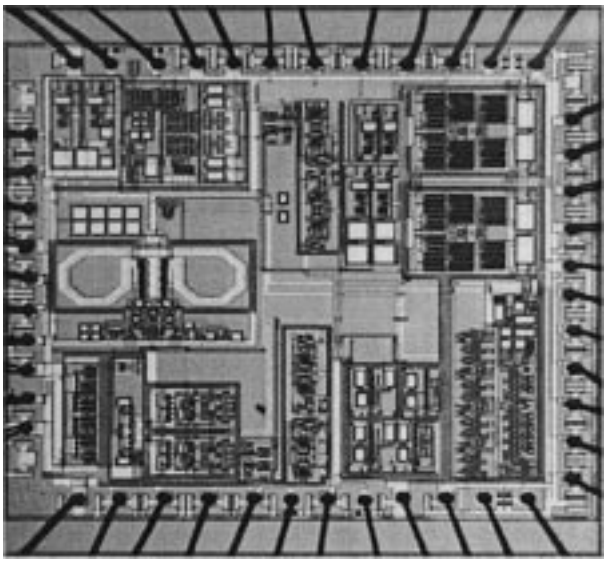

Fig. 4. Photomicrograph of a multiband SiGe transceiver including zero IF receiver and transmitter, I/Q mixers, prescaler, and 3.6-GHz VCO for GSM/digital communication system (DCS)/personal communication system (PCS).

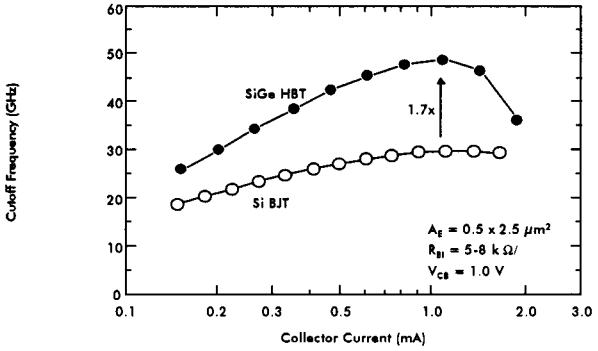

Fig. 5. Transition frequency of an Si and SiGe transistor with comparable geometry.

once again changing radio design. For example, the united performance of SiGe bipolar transistors (Figs. 4 and 5) with the massive digital integration of CMOS is opening the horizon for single-chip radio. Mobile broad-band communication will likely be enabled by new IC technologies such as silicon-on-insulator (SOI) CMOS. This technology improves the digital power consumption and the RF performance compared to regular CMOS. In addition, the principal issues for RFICs, parasitic coupling, and crosstalk, are simplified since all active devices are isolated naturally by silicon oxide. Similarly, in bipolar technology, the buried collector layer placed under the CMOS logic is a natural shield against substrate-coupled noise injection into the RF/analog blocks. silicon–carbide bipolar devices will be even faster than SiGe transistors and copper metallization together with low dielectric-constant insulators on silicon technology will further reduce the interconnect resistivity and the parasitic capacitance, respectively.

Despite a general optimism, many uncertainties remain. The SiGe and SOI technologies will be available, but will their cost match the requirements of BiCMOS RF–analog–digital radio

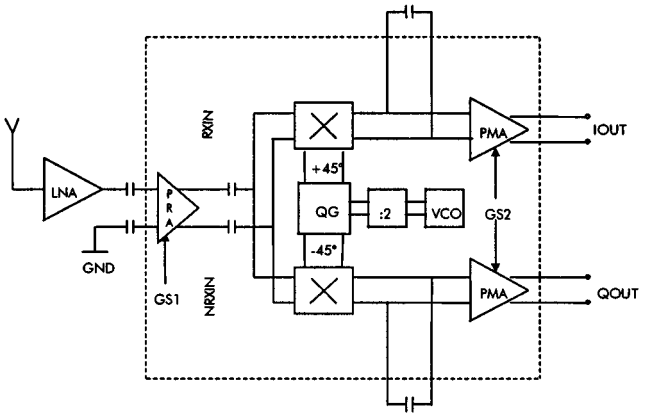

Fig. 6. Zero IF radio receiver in full production for GSM 900 since 1991 and for DCS 1800 for several years.

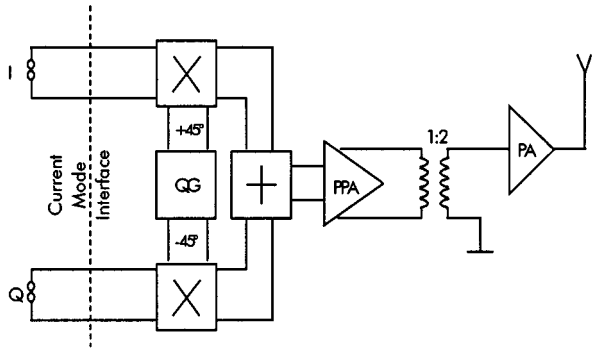

Fig. 7. Traditional Cartesian I/Q transmit modulator.

integration in the next few years? Will these or other technologies indeed prove to be the right ones? What are the appropriate new transceiver architectures? Are the current wireless standards suitable? Despite the absence of definite answers, we will now discuss several issues related to these questions.

IV. RFIC Technology Dilemma

Today, SiGe technology is available for virtually the same wafer cost as silicon RF-bipolar technology. The long-promised superior performance of SOI will become cost effective in "smart cut unibond wafers" and "thin oxide silicon implanted oxide (SIMOX)" technologies, competing in the low-power low-voltage CMOS market. The SOI wafer cost was an obstacle in the past for large-volume low-cost applications, but as we migrate to 1-V-supply voltages, the situation is changing. The major power saving in the reduced source and drain junction capacitance is now relevant compared to the loss in metal interconnect for large digital system integration. Also, the metal interconnect itself will be improved by the introduction of copper for low-resistivity and low-dielectric-constant insulators for reduced parasitic capacitors.

This plurality of technology innovations is creating a dilemma for research and development engineers and managers. During a single design cycle, the technology scene is changing so drastically that a conservative approach can create a major strategic mistake for the next product generation. Concurrent engineering on the product, the architectural and

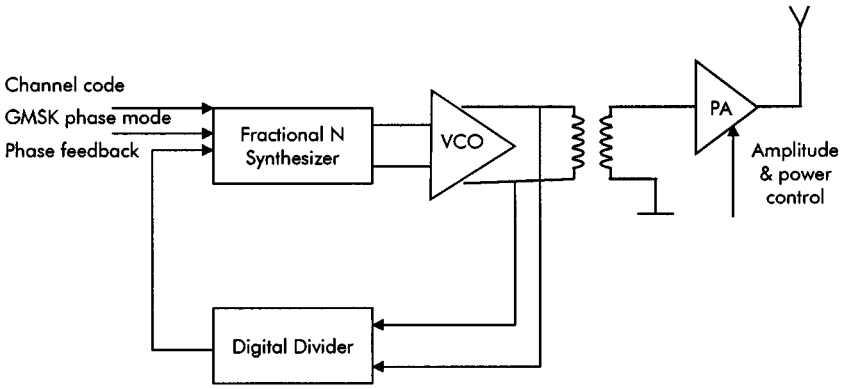

Fig. 8. Maximum digital zero I/Q modulator.

the technological level requires clear roadmaps to make sure that each of the research and engineering teams stay in line to achieve the common goal in the next product generation.

V. Transceiver Architecture

Several options are open for transceiver architectures and each manufacturer is likely to pick the one that fits the expertise of its own RF design team. Superheterodyne in-phase/quadrature (I/Q) receivers are widely used while some manufacturers have built up expertise in homodyne or direct conversion receivers. Direct conversion digital phones [2] have been in full production since 1991 [3] despite the objections of many conservative radio designers (Fig. 6). As will be shown further on, the dc-offset problem can be handled successfully. Direct conversion from RF to baseband avoids the need for discrete surface acoustic wave (SAW) filters as IF components. All filters for adjacent channels, blockers, and antialiasing filtering are realized as low-pass silicon analog ICs, applied routinely in speech processing for decades.

At the transmit side, a Cartesian I/Q modulator (Fig. 7) is generally used. However, mixer harmonics, image components, and other spurious signal components generated in the traditional I/Q transmitting (TX) modulator dictate the use of class-B or class-AB output stages for the PA. The resulting power efficiency is rather low, which is limiting the talk time. As the cellular system operators are reducing the cost of conversations, talk time will be the next strategic priority. The GSM modulation was chosen to allow the use of class-C amplifiers and uses a constant envelope Gaussian minimum shift-keying (GMSK) phase modulation.

In parallel with the Cartesian I/Q modulators, some manufacturers use polar modulators [4], popular in frequency shift-keying (FSK) systems for many years. Such a direct voltage-controlled oscillator (VCO) modulation method avoids the spurious components in the oscillator output spectrum. In this way, the linearity requirements of the PA are relaxed. This allows a design tradeoff in favor of the power-added efficiency [5].

A new trend in cellular transmitter architectures is applying modulation in the synthesizer loop (Fig. 8). The digital implementation of the channel stepper and the phase modulation in a fractional N loop are steps toward a "software radio." Such architecture is introduced to reduce the analog circuits and move functionality to digital blocks described using the very high level descriptive language (VHDL) code. This transition from analog to digital is a key element to further benefit from the cost reductions resulting from shrinking transistor dimensions.

VI. Transceiver Circuit Design

Since a few years, single-chip RF radio transceivers using a 5-V supply are phasing out in production for cellular applications. To reduce the number of batteries and the cost and the size of a portable cellular phone, new circuits for 3-V operation are in production. Although research results have been published for building blocks achieving a 2- and 1-V operation, the full integration of a complete 2.7-V battery transceiver, including prescaler, low-noise amplifier (LNA), receive and transmit mixers, baseband low-noise receive post mixer amplifiers (PMAs), RF pre-power amplifier (PPA), and local-oscillator (LO) VCO and Q phase shifter is still an outstanding challenge for today's commercial RF bipolar technologies. The Gilbert cell mixer is marginally applicable as the power supply is reduced to 2.7 V because it requires three levels of transistors in between the supply rails and a 1-V collector–emitter voltage is typically too low to achieve the peak f_T. In the circuits discussed later in this paper, a maximum of two stacked transistors between the rails is applied as design rule. The stages are capacitively coupled to achieve this goal. DC coupling between the stages makes it difficult to match the bias level at the output of each stage to the input of the next stage. Capacitive coupling is an easy solution to enable optimum dc-bias level conditions in each stage. However, capacitive coupling blocks the LF test signals. This is rendering the production testing more complex.

VII. Receiver Topology

A popular receiver architecture is a balanced Q demodulator, as shown in Fig. 6. By means of an input differential pair with emitter degeneration (see Fig. 9), the single-ended LNA output signal is converted to a balanced radio signal driving the mixers. Between the mixers outputs (see Fig. 10), external capacitors are connected to create a 300-kHz first-order *RC* low-pass filter suppressing the blocking levels at, for example, a distance of 3 MHz from the carrier. The $+45^{\circ}$ and the -45° LO signals are

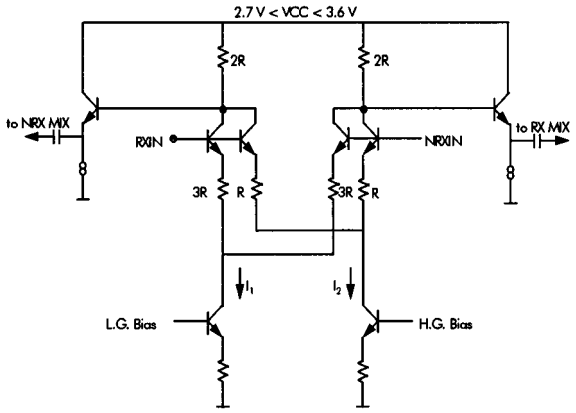

Fig. 9. Receiver preamplifier.

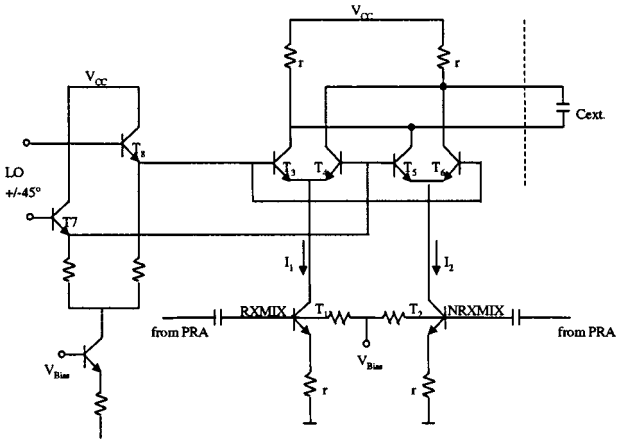

Fig. 10. Receive mixer.

generated by an on-chip *RC*/*CR* quadrature generator (QG). The noise figure of this receiver is 16 dB.

A. Receive Pre-Amplifier (PRA)

The purpose of the PRA (see Fig. 9) in the receiver is twofold: it provide 12-dB variable gain switching and boost the input signal by 8.5 dB in maximum gain mode. Two differential pairs connected in parallel to the two input pins RXIN and NRXIN is an elegant topology for this function. Driven from an external single-ended LNA, the radio signal hits the PRA on the RXIN input pin. The complementary pin NRXIN is capacitively coupled to ground. Activating the low gain (L.G.) or the high gain (H.G.) current sources allows to switch between the two gain modes. The emitter followers provide a low source impedance to drive the receive mixer input stage.

B. Receive Mixers

The PRA provides sufficient common mode rejection and present a balanced drive on the receiving (RX) mixer (see Fig. 10) transistors T_1 and T_2, which are capacitively coupled to the PRA. The four switching transistors (T_3–T_6) act as a balanced mixer on the current mode radio signal in I_1 and I_2. The bases of the switching mixer are dc coupled through the emitter followers T_7 and T_8 to the dc output level of the QGs. For good gain matching between the I/Q channel, the mixer transistors (T_3–T_6) are hard switched by the $\pm 45^{\circ}$ LO signal.

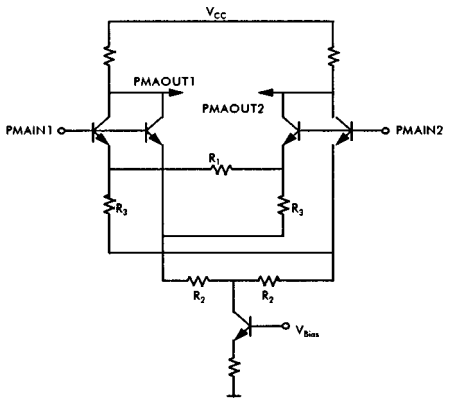

Fig. 11. Receiver PMA.

The mixers conversion gain is 0 dB. An external capacitor $(C\mathrm{ext})$ provides low-pass filtering to suppress the blocking signals and the adjacent channels and to avoid saturation in the bipolar circuitry. Further filtering is performed in the baseband CMOS automatic gain control (AGC) circuits and the final channel filtering is implemented with digital circuitry. To conclude the mixer discussion, we note that the common mode rejection of the PRA and the capacitive coupling of the balanced RX signal to the RXMIX and NRXMIX (Fig. 10) input make it possible to build a double balanced mixer using only two levels of n-p-n transistors between the supply rails.

C. Receive PMA

To cope with the noise level of the CMOS analog baseband signal processor, 16.5-dB gain in the PMA (see Fig. 11) is necessary to overcome the 40-dB noise figure of the CMOS circuitry. This brings the total maximum gain of the integrated receiver at 25 dB. The low base resistance in the SiGe transistors allows the design of a low-noise post-mixer amplifier in the RF front-end. A double asymmetrically degenerated differential pair (ADDP) maximizes the linear range of the PMA. Each of the ADDPs provides a maximum flat gain curve, one for the positive excursions of the RX signal, and one for the negative excursions. For a smooth cross over, cross coupling resistors are connected between the ADDPs.

D. Offset Compensation

DC offset is one of the major problems in zero IF receivers, and there is a common "belief" that it is almost impossible to solve. In this section, several offset compensation techniques are discussed. They are all based on the principle of "measure the offset up front, and subtract later on." Since most digital communication standards are based on a time-division multiple-access (TDMA) principle, the offset can be measured during the guardband in between two communications bursts.

In a downconverter, as shown in Fig. 6, each of the two signal paths can be considered as a multiplier. For example, the signal IOUT is ideally described by

$$V\mathrm{IOUT}(t) = A * Vlnain(t) * Vlo(t) \tag{1}$$

where A is the signal path gain, and $Vlnanin(t)$ and $Vlo(t)$ are, respectively, the RF input signal at the LNA input, and the LO

signal at one of the mixer inputs. However, in reality, this output signal is corrupted by real-life circuit-level nonidealities. If we limit ourselves to the influence of circuit offsets and distortions, (1) can be rewritten as

$$VIOUT(t) = a + b*Vlnain(t) + c*Vlo(t) + d*Vlnain^2(t) + e*Vlnain(t)*Vlo(t) + f*Vlo^2(t) + \cdots. \quad (2)$$

In this expression, the coefficient "c" represents the wanted downconversion of the RF input signal toward baseband. Indeed, multiplying the signal "$Vlnain(t)$" with "$Vlo(t)$" produces a wanted LF signal component plus a high-frequency signal component at the double of the RF frequency. The latter is filtered out by "$C\mathrm{ext}$" in Fig. 10.

The coefficients "b" and "c" represent the unwanted RF signal leakage and LO leakage, respectively. These nonidealities result in unwanted signal components at the mixer outputs. However, since these signals are high-frequency RF signals, they are suppressed by "$C\mathrm{ext}$" in Fig. 10.

Coefficient "f" represents a multiplication of the LO-signal with itself. This so-called self-mixing can e.g., be the result of a crosstalk from the LO signal to the LNA input, resulting in an LO signal being present at both mixer inputs. The result of this multiplication is a high-frequency signal at the double of the RF frequency, plus a dc signal. The former is suppressed by "$C\mathrm{ext}$," but the latter represents a dc-offset signal, which has to be canceled.

Similarly, coefficient "d" represents a multiplication of the RF input signal with itself. This multiplication can be due to signal leakage from the LNA input (or any other RF signal node) toward the LO. It can also be due to second-order harmonic distortion in the mixer. Again, this multiplication results in a harmless high-frequency signal, plus an offset signal component at dc. It should be noted that this dc offset depends on the square of the RF input signal. It is a *dynamic* offset, induced by all the RF input signal components present at the LNA input. It is to be noted that not only in-band RF signals can cause dynamic offset; most dynamic offset will be due to the large blocking signals out off the RF signal band of interest.

Finally, coefficient "a" represents a dc offset due to component mismatches. Component mismatches in the RF circuits before the mixer are not important, since the resulting dc offset can be easily filtered out by means of capacitive coupling. However, component mismatches in the mixer or in the baseband circuits after the mixer will result in dc-offset voltages that have to be compensated.

It should be noted that the offset voltages due to coefficients "a" and "f" are constant. They can be measured up front and filtered out afterwards. The offset due to coefficient "d" is signal dependent. In the presence of a *constant* blocker signal, the same principle of "measuring and compensating later on" can be applied. However, if the blocker amplitude is varying, only instantaneous measuring-and-compensating will work. Note also that the dynamic offset problem can be eased by means of differential circuits with low on-chip crosstalk and with a very high second-order intercept point (IP2).

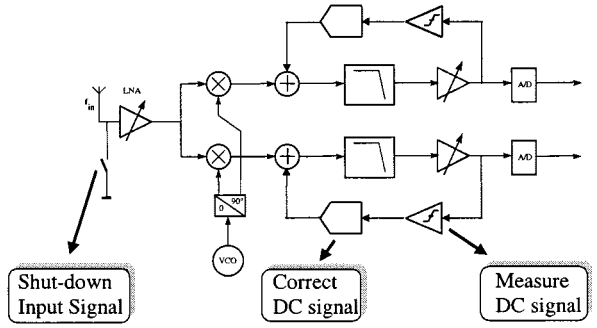

Fig. 12. Offset compensation by means of digital correction.

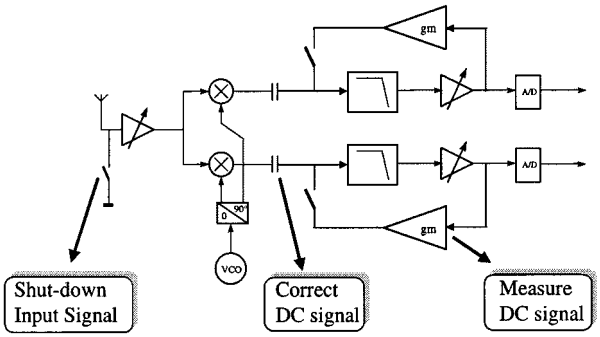

Fig. 13. Offset compensation by means of analog correlated double sampling.

In order to solve this dc-offset problem, let us first concentrate on those offset contributions that are *constant* during the time of one signal burst, i.e., the offset contributions due to coefficients "a" and "f" in (2). These offset voltages can be treated with a circuit, as depicted in Fig. 12. During the guardband in between two bursts, the input signal is shut down at the LNA input. This can be done, either with a real switch, or by placing the LNA in a power-down mode. Any remaining dc signals present further down in the signal path (e.g., at the inputs of the A/D converters) are unwanted dc-offset signal components that must be compensated for. These dc components are measured, and dc counteracting signals are injected at the mixer outputs by two D/A converters. The input words of the D/A converters are memorized in two digital registers for later use during the real signal bust. The remaining offset is primarily determined by the resolution of the D/A converters.

An alternative approach is depicted in Fig. 13. During the guardband, the offset voltages at the A/D converter inputs are compensated by analog feedback loops. By placing a charge on a series capacitor in the signal path, a dc countersignal is created to null the offset out. Later, before the signal burst, the switches in Fig. 13 are opened and, hence, the charges on these capacitors are kept constant. The accuracy of this "sample and hold" system is ultimately limited by the charge variations due to leakage currents.

These circuits do not compensate for the dynamic offset due to coefficient "d" in (2). Indeed, by short-circuiting the LNA input signal, all RF-signal induced offsets are not taken into account during the measurement and are, therefore, not compensated for. When the out-of-band RF signal levels can be considered as being constant during the duration of a signal burst, the circuits of Figs. 12 and 13 are also suited to compensate the

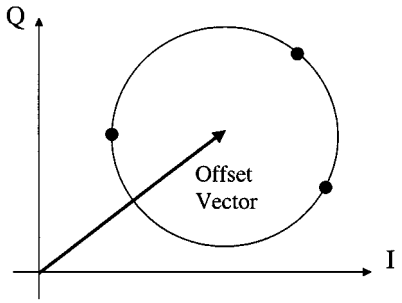

Fig. 14. Offset compensation by means of a circle fit.

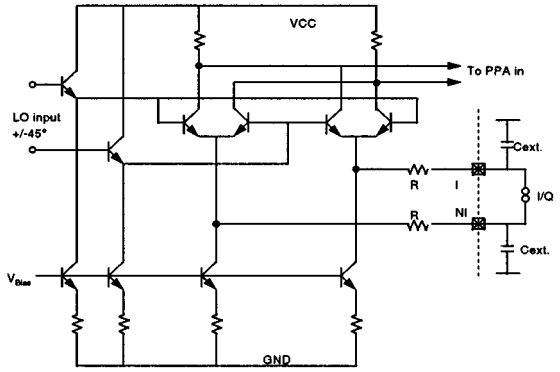

Fig. 15. Transmit RF mixer.

dynamic offset: once synchronization is found, the switches at the LNA inputs can be left open during the measurement phase. During the guardband, when the offset is measured, there is no wanted signal present at the LNA input. All dc signals further down in the signal paths are, hence, unwanted offset signals that have to be compensated for. These signals include the dynamic offset due to quasi-constant RF input signals.

Dynamic offsets due to nonconstant RF input signals cannot be cancelled by means of a "measure and compensate later on" approach. Such offsets can first be minimized by using circuits with a high IP2. If this is not sufficient, a real-time offset compensation schema has to be implemented. For example, for GSM (or any other standard with constant-envelope modulation), the dc offsets in the I and Q channels can be determined with a circle fitting from three noncoinciding symbols. This is shown in Fig. 14.

VIII. Transmitter Topology

The transmitter (see Fig. 7) is basically a zero IF single-sideband mixer followed by a PPA. A detailed schematic of the transmit mixer is shown in Fig. 15. In order to limit the number of stacked transistors to two, the baseband I and Q balanced inputs are current inputs, rather than voltage inputs. As a result, the only voltage swing on the mixers inputs are the LO signals delivered by the QG. The modulated collector currents of both the I and Q mixer enter a resistive summing node, which is driving the on-chip PPA. The PPA is delivering a 0-dBm output signal over a 1 : 2 transformer into the 50-Ω input of an external PA.

A. Transmit Mixer

As shown in Fig. 15, the transmitter uses two amplitude modulator (AM) cells driven by Q LO signals to obtain single-sideband (SSB) modulation. The AM mixer cells basically consist of two differential pairs and two emitter followers buffering the LO inputs. The baseband inputs are driven by floating current sources connected to the emitter nodes of the switching differential pairs. To separate the baseband circuitry from the RF switching circuits, a reverse RF filter is included between the base band I/Q input and the emitters of the switching transistors. The RF filter consists of an external capacitor $(C\mathrm{ext.})$ and an internal resistor R.

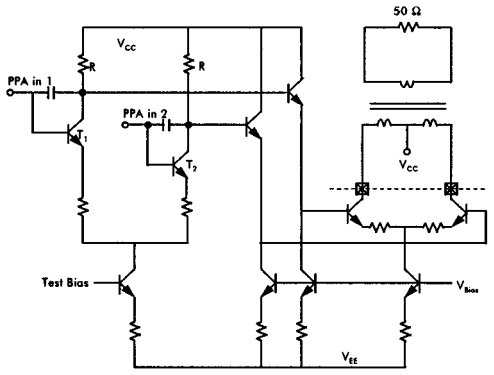

Fig. 16. PPA.

B. Transmit PPA

Except for the additional test circuits T_1, T_2, the PPA (see Fig. 16) consists of a basic differential pair and two emitter followers. The PPA operates in full class A.

To drive 0 dBm into the 50-Ω load through the 2 : 1 transformer, the swing on the open collectors is over 1.2 V_{PP}. The followers at the PPA input buffer the mixers. The result is three transistors between the 2.7-V supply rails. However, with the base inputs of the followers biased close to V_{CC}, the open collectors are biased at a V_{BE} reverse collector to base and the tail current source remains at $V_{\mathrm{CC}} - 2\ V_{\mathrm{BE}}$. As the test circuit is activated, rmT_1 and T_2 in Fig. 16 open an LF test path for the PPA and the TX mixers.

C. QG

The QG is shown in Fig. 17. It is designed to deliver two LO signals with a 90° phase difference accurate to within 1° phase error. This is possible using just an *RC* and a *CR* filter to obtain the $+45^\circ$ and -45° phase relation. The phase accuracy is well covered, but technology variations are the cause of an important variation of gain. To obtain the necessary gain matching of the I and the Q channel, limiting amplifiers are hard switched by the *RC*'s and the *CR*'s output voltages.

D. VCO

In the VCO schematic of Fig. 18, the transistors T_1 and T_2 are the gain elements. The emitters of T_1 and T_2 are ac coupled and the bias current is provided by the two current sources T_3 and T_4. The VCO resonator contains the inductors L_1, L_2 and the capacitors C_1, C_2. The base–emitter junction capacitors of transistors T_5 and T_6 act as varicaps with the control voltage (VCV) applied to the base. Fig. 19 shows the measured phase noise. When C_3 and C_4 are switched in, the VCO is jumping

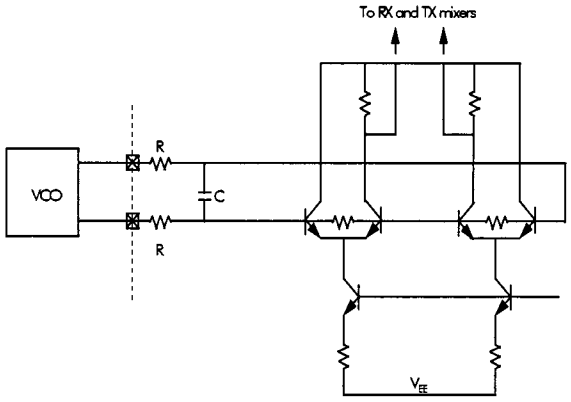

Fig. 17. $RC + 45^{\circ}$ phase shifter.

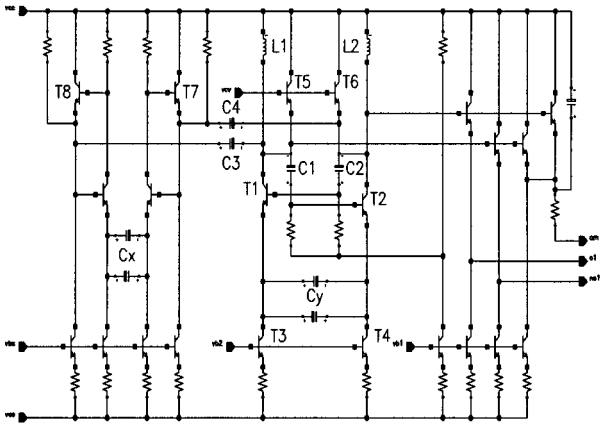

Fig. 18. Typical VCO circuit with integrated inductors.

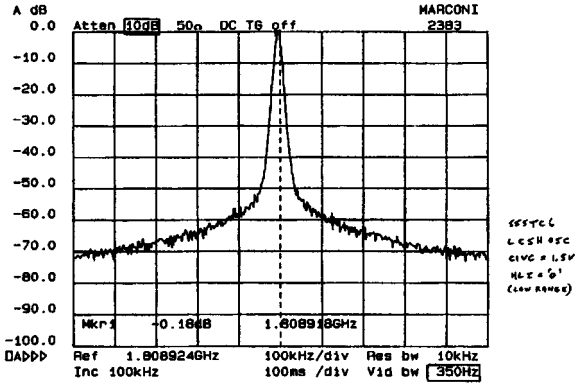

Fig. 19. Typical phase noise for an integrated VCO with spiral inductors.

from the RX to TX band. The phase noise at 10 and 100 kHz from the carrier is at -80 dBc/Hz, respectively, at 100 dBc/Hz.

IX. Circuit Interfaces

Circuit interfaces form an important aspect of large-scale radio integration. Traditional radio designers have created a 50-Ω culture with its impedance matching networks, standing wave ratios, s-parameters, power gains, noise figures, and signal levels measured in decibels and decibel/megawatt. With the exception of the s-parameter theory, which is extremely useful in the *modeling* of RF transistors, the other microwave concepts have little meaning for signal internally in an IC. For example, Gummel–Poon models for bipolar transistors and state of the art MM9, Berkeley simulation model (BSIM), or Emz Krummenacher, Vittoz (EKV) models for regular or SOI CMOS transistors work very well in RF simulations. S-parameters will remain the preferred way to measure the input impedance of the receiver and the output impedance of the transmitter. However, in fully integrated radio systems, these two quantities will be the only interfaces with the outside world. All other radio parts are internally in the silicon chip. It is quite difficult to measure RF signals on submicrometer lines internal to a chip. Therefore, RF measurements, which are forming the major skill of traditional radio engineers, are mapped to circuit simulations with a SPICE-like simulator. These simulations are another major skill for RFIC designers.

This explains why the new silicon RF-analog-ASIC designers speak a different language. They use simple words such as volts and amperes for signal levels and noise, rather than decibel/megawatt and noise figure. They use ohms for interface impedance because this is what the SPICE-like simulator displays on the screen of the design terminal. The 50-Ω interfaces standard no longer exist between integrated building blocks on a single chip. Moreover, an interface impedance of 50 Ω would be suboptimal anyway because silicon voltage noise is dominating over current noise at this low-impedance level.

50 Ω was a good impedance choice for discrete components with picofarad parasitic pin capacitance, but on IC chips, we have femtofarad parasitic capacitors. Likewise, the pins of low-cost plastic and ceramic packages are also well below 1 pF. Even the 50-ω standard for SAW filters and antennas will be questioned in the near future. The impedance transformer of the antenna changing the 300-Ω air interface to the 50-Ω SAW filter input impedance is just an additional cost for the product. Also, the optimum noise impedance of integrated silicon or SiGe LNAs is closer to 300 than 50 Ω anyway. Several discrete components on the radio receiver PCB can thus be saved if 300 Ω is used for SAW filter and antenna impedance.

The transmitter tradeoffs are different. Since a power of 2 W in a resistor of 50 Ω requires a voltage of 10 V $\cdot$ rms, impedance transformers with transformation factors in the order of ten are required to realize output amplifiers with power supply voltages below 3 V. A 300-Ω antenna impedance will require an even bigger transformer ratio to couple the IC output signal to the antenna. However, the issue remains that the current 50-Ω standard is neither a good match for the receiver, nor the transmitter. This shows that research is needed in this area to discover new tradeoffs and optimizations.

Despite all these arguments, the standard for external RF interfaces will remain 50 Ω at least for a while since measurement equipment, discrete filters, antenna production, and tradition will all push to maintain the current standard.

X. Designing for Minimum Power

The interconnections between RF building blocks remain an issue. Although the parasitic capacitances on a silicon IC are counted in femtofarads compared to picofarads on a PCB, the bandwidth on chip is limited by the interconnect

capacitance. This results from raising the impedance level to reduce the power consumption. In discrete component radios, this problem was solved by selective *LC* tuning. However, the cellular phone market requires multistandard and multiband operation. Therefore, in order to keep the circuits wide-band, we have to cut the interconnect length to the minimum possible by optimum layout floor planning. Auto-routing tools are not always applicable and, as the integration level increases, careful hand crafted layout is a must in the RF sections of the chip.

XI. Integrated Inductors

The integration of spiral inductors in silicon RFIC technology has been the subject of many recent studies and developments. The best reported quality (Q) factors are between 10–20, depending on the technology. In standard silicon bipolar and CMOS, the Q factor is determined by the metal resistivity and by the substrate eddy current losses. Many technology modifications can be applied to improve this Q factor, such as a thick oxide layer under the inductor, trench isolation to cut the eddy currents, a gold or copper interconnect layer, or a thick aluminum interconnect layer. Other manufacturers place the inductor on top of the chip passivation, hereby minimizing the substrate parasitic capacitance. This allows to realize the inductor in a thick electroplated copper or gold layer.

The area occupied by on-chip inductors is about three orders of magnitude larger than the area occupied by a transistor. Moreover, integrated inductor modeling is difficult and is typically limited to an accuracy below 10%. However, compared to discrete inductors, their reproducibility is a lot better in production. Two to three design iterations are usually sufficient to meet the desired values. Passive RF *RLC* circuits are becoming feasible in silicon IC technology, but the integration of duplex filters for cellular phones still requires Q factors that are an order of magnitude higher than what is available today.

In addition to filters, fully integrated VCOs use on-chip inductors. The VCO phase noise is directly determined by the quality factor of the resonator tank, which is primarily dominated by the Q factor of the inductor. A typical bipolar VCO circuit example is shown in Fig. 15. For a GSM handset, the performance of such a VCO is marginal (Fig. 16), and for a GSM base station, the standard silicon inductors are still far too noisy.

XII. Modeling and Simulations

Since in-circuit RF measurements are very difficult or even unfeasible, simulations with accurate models are key for RFIC designers. The plurality of bias conditions applied to the integrated RF transistors requires the flexibility of a SPICE-like simulator. In the past, the integration level of RFICs was limited by modeling and simulation time constraints, but today, this situation is improving. On one hand, complex simulations are benefiting from the ever-increasing calculation power of modern work stations. On the other hand, dedicated RF simulators are becoming available. These simulators allow to analyze signals with a large variety of time constants in a reasonable time. Furthermore, these simulators allow to analyze nonlinear steady-state noise, important, for example, in mixers.

For many years, RF semiconductor foundries have perfected their tools and software for transistor RF modeling, parameter prediction, and parameter extraction. This methodology is applied even for a new technology under development. The devices are measured on wafers and well-known deembedding procedures are applied to compensate for the parasitics of the bonding pads, the probes, and the measurement equipment.

For example, some suppliers provide accurate package models, and soon, flip-chip technology will reduce the chip interface parasitic components to a bare minimum. Still, complex phenomena such as the VCO pulling by a 2-W PA on the same chip are very difficult to simulate accurately. For such problems, the solutions are more likely to come from novel architectures rather than from design tools or technology advancements. For example, operating the VCO and PA in different bands of the spectrum is a good option. This approach has the added advantage of lowering the VCO phase noise. If we double or quadruple the frequency of the resonator and we use subsequent frequency division to obtain the cellular carrier frequency, we get a dual benefit. First, the inductor Q factor is increased as the reactive impedance goes up relative to the metal line resistivity and, second, frequency division reduces phase noise by 6 dB for each division by two.

XIII. Role of Intellectual Property

An important aspect of any ASIC design is intellectual property (IP) transfer. Exchange and cross licensing of IP is the key to speeding up the process of full radio integration. In the area of RFICs, we have a win–win situation. The advanced silicon technology is mature and available for full radio integration. It is time to merge digital, analog, and RF on a single chip. However, the limited availability of RF-silicon and ASIC designers worldwide is the bottleneck. Exchange of building blocks and design effort sharing are beneficial for all cooperative partners.

XIV. Conclusion

Despite ten years of pioneering work and many circuit advances, the RF ASIC field still offers room for expansion. This expansion is driven by new silicon IC technology capabilities and challenging product requirements. While radio large-scale integration in silicon technology has been the area of main interest in the past ten years, the next crucial topic is mixed RF-analog–digital integration. The main hurdles in this development will come from the isolation between building blocks, the on-chip interference, and crosstalk via the supply lines and parasitic elements. This problem is similar to mixed analog–digital designs. New tools for system and circuit level analysis/synthesis will be employed, but architecture and system innovations will be the driving force for further growth in silicon-integrated radio.

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